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DSD Synthesis Based on Variable Intersection Graphs  
*Vinicius Callegaro, Mayler Martins, Renato Ribas and Andre Reis*

Asynchronous Circuits and a Pipeline Controller Design: A review  
*Frederico Butzke*

Automatic Design of an OTA based on Particle Swarm Optimization  
*Robson Domanski, Alessandro Girardi and Leonardo Tomazine*

Improved Logic Synthesis for Memristive Stateful Logic Using Multi-Memristor Implication  
*Felipe Marranghello, Vinicius Callegaro, Mayler Martins, Andre Reis and Renato Ribas*

A Study on the Automatic Synthesis of Layout with ASTRAN using FreePDK 45nm  
*Gisell Moura, Adriel Ziesemer and Ricardo Reis*

Implementing Transistor Folding Technique in ASTRAN CAD Tool  
*Gustavo Smaniotto, Leomar Rosa Jr., Felipe Marques, Adriel Ziesemer Jr. and Matheus Moreira*

Gate Clustering on Post Technology Mapping Netlist  
*Calebe Conceicao and Ricardo Reis*

**Sessão 2A: Design Automation Tool - II - Chair:**

07/05/2014 - 16:30

Iterative Mapping Approach Using Simulated Annealing Technique on FlexMap Tool  
*João Júnior Da Silva Machado, Julio Saraçol Domingues Junior, Leomar Soares Da Rosa Junior and Felipe de Souza Marques*

Evaluating Non-Series-Parallel Cells Concerning Area and Wirelength Aspects
Maicon Cardoso, Felipe Marques and Leomar Rosa Junior

Series-Parallel Switch Network Generator for Read-Once Functions
Lucas Carraro, Vinicius Callegaro, Renato Ribas and André Reis

Non-Series-Parallel Network Catalog Generator
Réges Eduardo Júnior Oberderfer, Vinicius Callegaro, André I. Reis and Renato P. Ribas

Study on the Potential Simplification of a Customized Library Approach for Logical Synthesis
Luciana Mendes Da Silva, Guilherme Bontorin and Ricardo Reis

Applying Poisson equation with a quadratic approach to standard cell placement
Mateus Fogaça, Guilherme Flach, Marcelo Johann, Paulo Francisco Butzen and Ricardo Reis

Jezz: An Effective Legalization Algorithm for Minimum Displacement
Julia Puget, Guilherme Flach, Marcelo Johann and Ricardo Reis

Comparison among Algorithms for the Identification of Adaptive Memory Polynomial Predistorter Models
Luis Schwartz and Eduardo Goncalves De Lima

A Simplified Bi-dimensional Memory Polynomial Model for the Predistortion of Dual-band RF PAs
Otávio Augusto Da Paixão Riba and Eduardo Goncalves De Lima

MCML Standard Cell Library: topologies analysis
Bruno Canal, Paulo Butzen, Renato Ribas and Eric Fabris

Design of a Two-Stage Fully Differential Amplifier Through an Optimization-Based Methodology
Arthur Oliveira, Paulo Comassetto de Aguirre and Alessandro Girardi
A 120s-time-constant 2nd order Butterworth low-pass Gm-C filter based on a novel Reverse Cascode topology

Rafael Sanchotene and Cesar Rodrigues

Neutrons Sensitivity Evaluation of Parallel Processors and Heterogeneous Systems

Vinícius Fratin Netto, Daniel A. G. Oliveira, Paolo Rech and Ricardo Reis

Testing a Fully Differential Amplifier for Catastrophic and Parametric Faults by Reusing the Common Mode Feedback

Isis Bender, Guilherme Cardoso, Arthur Oliveira, Lucas Severo, Alessandro Girardi and Tiago Balen

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A Method for Hardware and Software Comparison of CRC-16 and FDCT Functions

Rafael C. Schneider and Fábio L. L. Ramos

Instruction-driven Timing CPU Model For Many-Core Systems

Felipe Rosa, Ricardo Reis and Luciano Ost

Izhikevich’s Simple Model on FPGA

Vitor Bandeira, Vivianne L. Costa, Guilherme Bontorin and Ricardo Reis

Cooperative Cu-Level Rate Control Scheme for HEVC

Volnei Mazui, Bruno Vizzotto and Sergio Bampi

A Hardware Architecture for an HEVC Motion Compensation Luminance Interpolator

Wagner Penny, Marcelo Porto, Luciano Agostini and Bruno Zatt

Coupling the ARISE Tool to a SparcV8 Processor

Michael Jordan and Mateus Rutzig

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Alexandra Lackmann Zimpeck, Cristina Meinhardt and Ricardo Reis
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A Near-Threshold Standard Cell Library Design Methodology for 0.6µm Technology Process
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Small Delay Defect Investigation in Critical Path Delay with Multiple TSVs
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